What is claimed is:

1. A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having a first major surface and a second major surface;

a second semiconductor layer of a second conductivity type on the first major surface of the first semiconductor layer, the second semiconductor layer being doped more heavily than the first semiconductor layer;

a third semiconductor layer of the first conductivity type on the second major surface of the first semiconductor layer, the third semiconductor layer being doped more heavily than the first semiconductor layer; and

a fourth semiconductor layer of the first conductivity type extending across the first semiconductor layer, the fourth semiconductor layer being spaced apart from the second semiconductor layer and the third semiconductor layer, the fourth semiconductor layer being doped more heavily than the first semiconductor layer.

2. The semiconductor device according to Claim 1, wherein the fourth semiconductor layer is formed uniformly across the first semiconductor layer.

3. The semiconductor device according to Claim 1, wherein the fourth semiconductor layer comprises a plurality of regions.

4. The semiconductor device according to Claim 1, wherein the impurity concentration in the portion of the first semiconductor layer between the second semiconductor layer and the fourth semiconductor layer is lower than the impurity concentration in the portion of the first semiconductor layer between the third semiconductor layer and the fourth semiconductor layer.

5. A semiconductor device comprising:

a drift layer of a first conductivity type having a first major surface and a second major surface;

an anode layer of a second conductivity type on the first major surface of the drift layer, the anode layer being doped more heavily than the drift layer;

a cathode layer of the first conductivity type on the second major surface of the drift layer, the cathode layer being doped more heavily than the drift layer; and

a buffer layer of the first conductivity type extending across the drift layer, the buffer layer being spaced apart from the anode layer and the cathode layer, the buffer layer being doped more heavily than the drift layer.

6. The semiconductor device according to Claim 5, wherein the buffer layer is formed uniformly across the first semiconductor layer.

7. The semiconductor device according to Claim 5, wherein the buffer layer comprises a plurality of regions.

8. The semiconductor device according to Claim 5, wherein the impurity concentration in the portion of the drift layer between the anode layer and the buffer layer is lower than the impurity concentration in the portion of the drift layer between the cathode layer and the buffer layer.

9. The semiconductor device according to Claim 5, wherein the shortest distance X_1 from the pn-junction between the anode layer and the drift layer to the edge of the buffer layer on the side of the anode is expressed by the following relational expression:

$$0.3 \leq X_1/\{(BV\ \varepsilon_s)/q[(J_F/q\ \nu_{sat}) + N_D]\}^{1/2} \leq 1.6,$$

where BV is the breakdown voltage of the semiconductor device, ε_s is the dielectric permittivity of the semiconductor, q is the elementary charge quantity, J_F is the rated current density of the semiconductor device, ν_{sat} is the carrier saturation velocity, and N_D is the concentration of the impurity of the first conductivity type in the drift layer.

10. The semiconductor device according to Claim 5, wherein the shortest distance X_1 from the pn-junction between the anode layer and the drift layer to the edge of the buffer layer on the side of the anode is expressed by the following relational expression:

$$0.8 \leq X_1/\{(BV\ \varepsilon_s)/q[(J_F/q\ \nu_{sat}) + N_D]\}^{1/2} \leq 1.2,$$

where BV is the breakdown voltage of the semiconductor device, ε_s is the dielectric permittivity of the semiconductor, q is the elementary charge quantity, J_F is the rated current density of the semiconductor device, ν_{sat} is the carrier saturation velocity, and N_D is the concentration of the impurity of the first conductivity type in the drift layer.

11. The semiconductor device according to Claim 5, wherein the thickness Y_1 of the buffer layer and the average impurity concentration N_{D2} of the buffer layer are related with each other by the following relational expression:

$$Y_1/\{[X_1^2 + 2\varepsilon_s\ (V_{CC} + V_{PT})/q\ N_{D2}]^{1/2} - |\ X_1\} \leq 2,$$

where X_1 is the shortest distance from the pn-junction between the anode layer and the drift layer to the edge of the buffer layer on the side of the anode, V_{CC} is the half value of the breakdown voltage of the semiconductor device, V_{PT} is the voltage, at which the depletion layer contacts the buffer layer of the first conductivity type, ε_s is the dielectric permittivity of the semiconductor, and q is the elementary charge quantity.

12. The semiconductor device according to Claim 9, wherein the thickness Y_1 of the buffer layer and the average impurity concentration N_{D2} of the buffer layer are related with each other by the following relational expression:

$$Y_1/\{[X_1^2 + 2\varepsilon_s\ (V_{CC} + V_{PT})/q\ N_{D2}]^{1/2} - |\ X_1\} \leq 2,$$

where X_1 is the shortest distance from the pn-junction between the anode layer and the drift layer to the edge of the buffer layer on the side of the anode, V_{CC} is the half value of the breakdown voltage of the semiconductor device, V_{PT} is the voltage, at which the depletion layer contacts the buffer layer of the first conductivity type, ε_s is the dielectric permittivity of the semiconductor, and q is the elementary charge quantity.

13. The semiconductor device according to Claim 10, wherein the thickness Y_1 of the buffer layer and the average impurity concentration N_{D2} of the buffer layer are related with each other by the following relational expression:

$$Y_1/\{[X_1^2 + 2\varepsilon_s (V_{CC} + V_{PT})/q\, N_{D2}]^{1/2} - X_1\} \leq 2,$$

where X_1 is the shortest distance from the pn-junction between the anode layer and the drift layer to the edge of the buffer layer on the side of the anode, V_{CC} is the half value of the breakdown voltage of the semiconductor device, V_{PT} is the voltage, at which the depletion layer contacts the buffer layer of the first conductivity type, ε_s is the dielectric permittivity of the semiconductor, and q is the elementary charge quantity.

14. The semiconductor device according to Claim 7, wherein the buffer layer comprises a plurality of selectively formed island-shaped regions.

15. The semiconductor device according to Claim 7, wherein the buffer layer comprises a plurality of selectively formed stripe-shaped regions.

16. A semiconductor device comprising:

a bulk wafer comprising a first drift layer of a first conductivity type, the bulk wafer having a first major surface and a second major surface;

a buffer layer of the first conductivity type on the first major surface of the bulk wafer, the buffer layer being doped more heavily than the first drift layer by implanting an impurity of the first conductivity type;

a second drift layer of the first conductivity type epitaxially grown on the buffer layer, the second drift layer being doped more lightly than the buffer layer;

an anode layer formed by implanting an impurity of a second conductivity type into the second drift layer;

an anode electrode on the anode layer;

a cathode layer on the surface of the bulk wafer exposed by grinding back the bulk wafer for a predetermined depth from the second major surface thereof, the cathode layer being doped more heavily than the first drift layer by implanting an impurity of the first conductivity type; and

a cathode electrode on the cathode layer.

17. A method of manufacturing a semiconductor device, the method comprising the steps of:

implanting an impurity of a first conductivity type into the first major surface of a bulk wafer comprising a first drift layer of the first conductivity type to form a buffer layer of the first conductivity type doped more heavily than the first drift layer;

growing epitaxially a second drift layer of the first conductivity type on the buffer layer, the second drift layer being doped more lightly than the buffer layer;

implanting an impurity of a second conductivity type into the second drift layer to form an anode layer;

forming an anode electrode on the anode layer;

grinding back the bulk wafer from the second major surface thereof to remove the portion of the bulk wafer for a predetermined depth from the second major surface;

implanting an impurity of the first conductivity type to the surface of the bulk wafer exposed by the grinding back to form a cathode layer doped more heavily than the first drift layer; and

forming a cathode electrode on the cathode layer.